6. (Amended) A method of forming a transistor, comprising:

forming a first gate dielectric layer on a semiconductor substrate;

forming a first conductivity type semiconductor layer on top of the first gate dielectric layer;

selectively removing a portion of the first conductivity type semiconductor layer to expose the first gate dielectric, the portion defining a first conductivity type well region;

forming a first conductivity type semiconductor well in the first conductivity type well region;

removing the first gate dielectric layer in the first conductivity type well region to expose a portion of the first conductivity type semiconductor well;

forming a second gate dielectric layer over the exposed portion of the first conductivity type semiconductor well, the second gate dielectric layer being adapted for operation with a second conductivity type gate material;

depositing a second conductivity type semiconductor material on the second gate dielectric layer and forming a second conductivity type gate from the second conductivity type semiconductor layer; and

forming source/drain regions adjacent the gate.

13. (Amended) A method of forming pair of transistors, comprising:

forming a second conductivity type semiconductor well in a semiconductor substrate;

forming a gate dielectric layer on the semiconductor substrate;

forming a first conductivity type semiconductor layer on top of the gate dielectric layer, over the second conductivity type semiconductor well;

selectively removing a portion of the first conductivity type semiconductor layer to expose the gate dielectric layer, the portion defining a first conductivity type well region;

forming a first conductivity type semiconductor well in the first conductivity type well region;

modifying the gate dielectric layer in the first conductivity type well region, the modified gate dielectric being adapted for operation with a second conductivity type gate material;

depositing a second conductivity type semiconductor layer on the modified gate dielectric layer;

patterning and forming gates from the first conductivity type semiconductor layer and the second conductivity type semiconductor layer; and

forming source/drain regions adjacent the gates.

18. (Amended) A method of forming a pair of transistors, comprising:

forming a second conductivity type semiconductor well in a semiconductor substrate;

forming a first gate dielectric layer on the semiconductor substrate;

forming a first conductivity type semiconductor layer on top of the first gate dielectric layer, over the second conductivity type semiconductor well;

selectively removing a portion of the first conductivity type semiconductor layer to expose the first gate dielectric, the portion defining a first conductivity type well region;

forming a first conductivity type semiconductor well in the first conductivity type well region;

removing the first gate dielectric layer in the first conductivity type well region to expose a portion of the first conductivity type semiconductor well;

forming a second gate dielectric layer over the exposed portion of the first conductivity type semiconductor well, the second gate dielectric layer being adapted for operation with a second conductivity type gate material;

depositing a second conductivity type semiconductor layer on the second gate dielectric layer;

patterning and forming gates from the first conductivity type semiconductor layer and the second conductivity type semiconductor layer; and

forming source/drain regions adjacent the gates.